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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/557,164	04/25/2000	William J. Dally	2789.2004-001	9280

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/557,164	DALLY ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-65 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1-17,31-47 and 65 is/are allowed.

6)☒ Claim(s) 18-30 and 48-64 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 4/19/06 in which claims 1-66 are pending. The applicant's amendments have bee fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 18, 50 and 66 are rejected under 35 U.S.C. 102(b) as being anticipated by Joo et al U.S. Patent No 5,525,935.

As per claims 18, 50 and 66, Joo et al teaches a data transmitter comprising: a data input (see fig.2 element NRZ data); a bit clock (see fig.2 element REFCP); a rise or fall transition time control circuitry for receiving the data input and providing a controlled data signal, having a transition time to be proportional to bit time of the bit clock (see abstract and col.3, lines 9-42 and col.4, lines 50-67 and col.5, lines 25-40).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19-27 and 51-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joo et al in view of Regula U.S. Patent No 6,885,670 B1.

As per claims 19, and 51, Joo et al teaches all the features of the claimed invention except a clock signal applied the delay elements and different delays are applied to the data input.

Regula teaches a clock signal (see fig.19a element 1905) applied the delay elements and different delays are applied to the data input (see fig.19 elements 1907, 1909 and col.47, lines 15-55).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Regula into Joo as to allow routing decisions to be made so quickly which would represent a significant advance in the state of the art as taught by Regula (see col.47, lines 47-50).

As per claims 20-21 and 52, Regula teaches a plural driver circuits (see col.6, lines 56-58). Furthermore implementing such drivers into Joo would have been obvious to ne skilled in the art as to facilitate communication between different nodes as taught by Regula (see col.6, lines 55-67).

As per claims 22 and 54, Joo and Regula in combination would teach load capacitance as to allow routing decisions to be made so quickly which would represent a significant advance in the state of the art and facilitate communication between different nodes.

As per claim, 53 Joo and Regula in combination would teach CMOS inverters as to allow routing decisions to be made so quickly which would represent a significant advance in the state of the art and facilitate communication between different nodes.

As per claims 27 and 59, Joo and Regula in combination would teach a voltage supply to control delay of the delay elements as to allow routing decisions to be made so quickly which would represent a significant advance in the state of the art and facilitate communication between different nodes.

As per claims 30 and 62, Joo and Regula in combination would teach voltage supply compensate for environmental changes in delay as to allow routing decisions to be made so quickly which would represent a significant advance in the state of the art and facilitate communication between different nodes.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 23-26, 28-29, 31-32, 55-58, 60-61, 63-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joo et al in view of Regula U.S. Patent No 6,885,670 B1 and in further view of O' Sullivan U.S. Patent No 6,259,755 B1.

As per claims 23 and 55 Joo and Regula in combination teach all the features of the claimed invention except parallel delay elements.

O' Sullivan et al teaches parallel delay elements (see fig.15).

It would have been obvious to one of ordinary skill in the art to implement the teaching of O' Sullivan into Joo and Regula as to accurately synchronize the input time delayed data with clock data.

As per claims 24-25, 56-57 Regula teaches a plural driver circuits (see col.6, lines 56-58). Furthermore implementing such drivers into the combination of Joo and O' Sullivan would have been obvious to ne skilled in the art as to facilitate communication between different nodes as taught by Regula (see col.6, lines 55-67).

As per claim 53, Joo and Regula and O'Sullivan et al in combination would include CMOS inverters as to enhance the transmitter capability in generating equal voltage supply to each driver

As per claims 26 and 54, 58, the data transmitter of Joo and Regula and O'Sullivan et al in combination would include load capacitance as to enhance the transmitter capability in generating equal voltage supply to each drivers.

As per claims 28-29, 31-32, 60-61, 63-64 Joo and Regula teach all the features of the claimed invention except a circuit to control power supply voltage to the delay elements the circuit comprising: a first and second delay elements (see fig.15), each receiving a common clock signal and a phase comparator (see fig.15 elements PFD) which compares the outputs of the first and second delay elements and control a supply

voltage applied to the first and second delay elements to control phase difference of the outputs.

O' Sullivan et al teaches a circuit to control power supply voltage to the delay elements the circuit comprising: a first and second delay elements (see fig.15), each receiving a common clock signal and a phase comparator (see fig.15 elements PFD) which compares the outputs of the first and second delay elements and control a supply voltage applied to the first and second delay elements to control phase difference of the outputs (see col.11, lines 19-25).

It would have been obvious to one of ordinary skill in the art to implement the teaching of O' Sullivan into Joo and Regula as to accurately synchronize the input data with clock data.

Allowable Subject Matter

Claims 1-17, 31-47 and 65 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: a data output that combines the delayed data signals, a rise or fall transition time of the data output being determined by different delays applied to the data input wherein the rise or fall transition Time of the data output signal is greater than the rise or fall transition time of the data input as recited in claim 1, 33 and 65.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishibashi et al U.s. Patent No 5,347,233 teaches PLL circuit.

Millar U.S. Patent No 6,337,590 B1 teaches a Digital delay locked loop.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2611

4/28/06

EMMANUEL BAYARD
PRIMARY EXAMINER